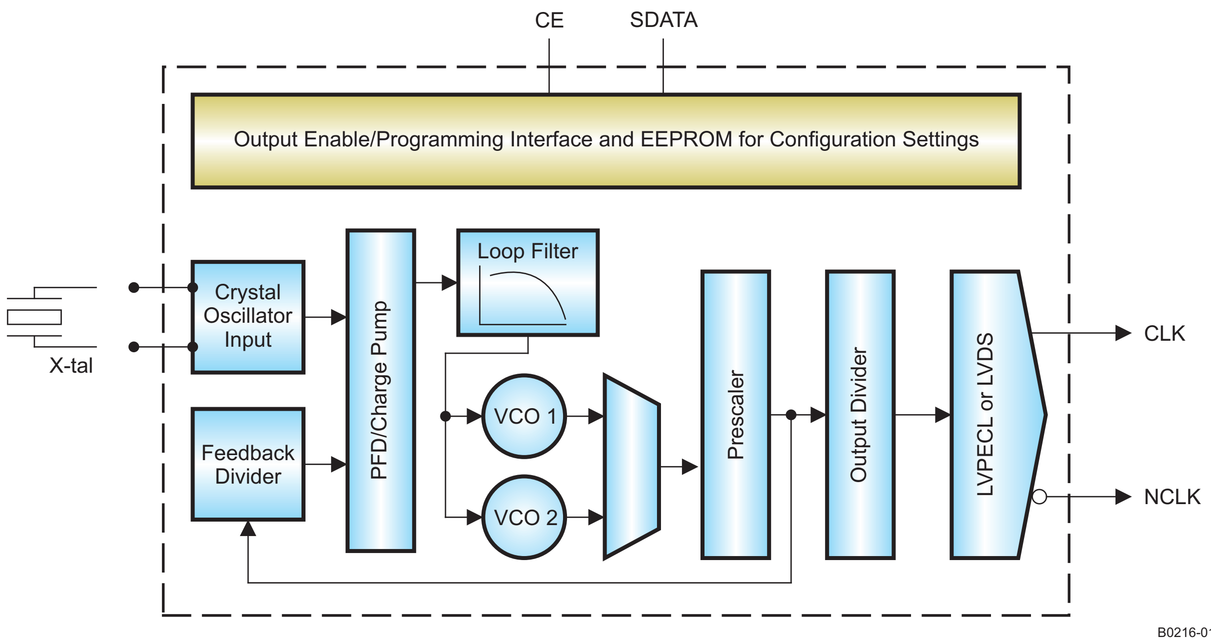
Fully Integrated Wide-Range, Low-Jitter, Crystal-Oscillator Clock Generator

FEATURES

- **Single 3.3-V Supply**
- **High-Performance Clock Generator Incorporating Crystal-Oscillator Circuitry With Integrated Frequency Synthesizer**
- **Low-Output Jitter, as Low as 380 fs (rms Integrated Between 10 kHz–20 MHz)**
- **Low Phase Noise at High Frequency; at 708 MHz It Is Less Than –109 dBc/Hz at 10-kHz and –146 dBc/Hz at 10-MHz Offset From the Carrier**
- **Supports Crystal Frequencies Between 27.35 MHz to 38.33 MHz**
- **Output Frequency Ranges From 10.9 MHz up to 766.7 MHz and From 875.2 MHz up to 1175 MHz**
- **Low-Voltage Differential Signaling (LVDS) Output, 100-Ω Differential Off-Chip Termination, 10.9-MHz to 400-MHz Frequency Range**
- **Differential Low-Voltage Positive Emitter-Coupled Logic (LVPECL) Output, 10.9-MHz to 1.175-GHz Frequency Range**
- **Two Fully Integrated Voltage-Controlled Oscillators (VCOs) Support Wide Output Frequency Range**
- **Fully Integrated Programmable Loop Filter**
- **Typical Power Consumption 240 mW in LVDS Mode and 300 mW in LVPECL Mode**
- **Chip-Enable Control Pin**
- **Simple Serial Interface Allows Programming After Manufacturing**
- **Integrated On-Chip Non-Volatile Memory (EEPROM) to Store Settings Without the Need to Apply High Voltage to the Device**
- **Die or QFN24 Package**
- **ESD Protection Exceeds 2 kV HBM**
- **Industrial Temperature Range –40°C to 85°C**

APPLICATIONS

- **Low-Cost, High-Frequency Crystal Oscillator**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The CDCE421 is a high-performance, low-phase-noise clock generator. It has two fully integrated, low-noise, LC-based voltage controlled oscillators (VCOs) that operate in the 1.750-GHz–2.350-GHz frequency range. It has an integrated crystal oscillator that operates in conjunction with an external AT-cut crystal to produce a stable frequency reference for the PLL-based frequency synthesizer.

The output frequency (f_{out}) is proportional to the frequency of the input crystal (f_{xtal}). The prescaler divider, feedback divider, output divider, and VCO selection are what set (f_{out}) with respect to (f_{xtal}). For a desired frequency (f_{out}), look in Table 1 and find the corresponding settings in the same row. Use Equation 1 to calculate the exact crystal oscillator frequency needed for the desired output.

$$f_{xtal} = \left(\frac{\text{OutputDivider}}{\text{FeedbackDivider}}\right) \times f_{out} \quad (1)$$

Output divider[(1)] = 1, 2, 4, 8, 16, or 32

Feedback divider[(2)] = 12, 16, 20, or 32

(1)Output divider and feedback divider should be from the same row in Table 1.

(2)Feedback divider is set automatically with respect to the prescaler setting in Table 1.

A high-level block diagram of the CDCE421 is shown in Figure 1.

The CDCE421 supports one differential LVDS clock output or one differential LVPECL output.

All device settings are programmable through a Texas Instruments proprietary simple serial interface.

The device operates in a 3.3-V supply environment and is characterized for operation from –40°C to 85°C.

The CDCE421 is available in die form or in a QFN-24 package.

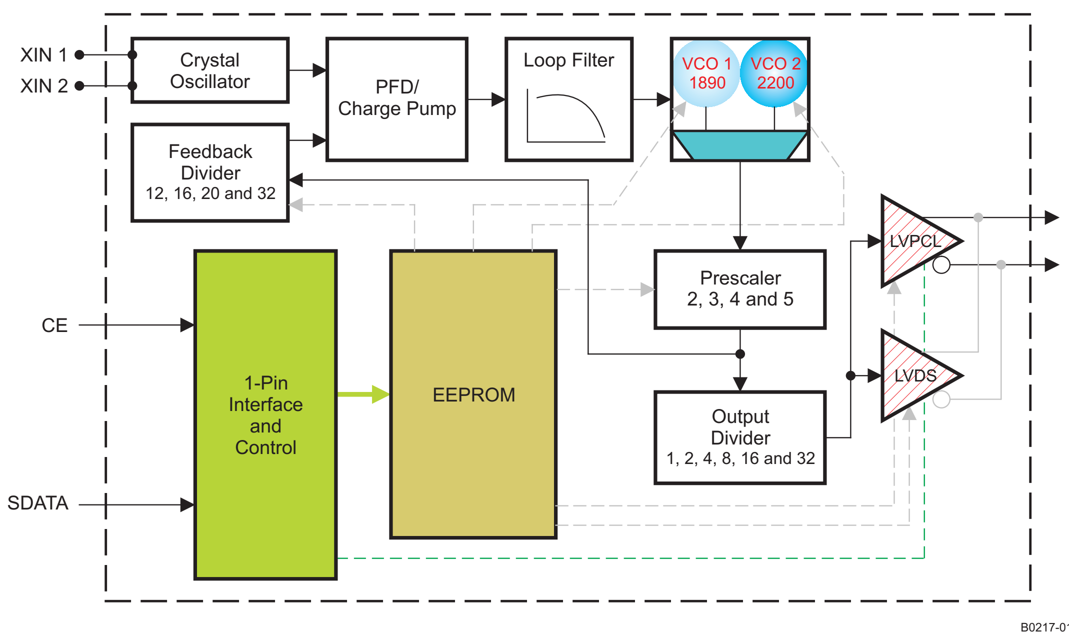


Figure 1. High-Level Block Diagram of the CDCE421

In the CDCE421, the feedback divider is set automatically with respect to the prescaler setting. The product of the prescaler and the feedback divider will be either 60 or 64, as shown in Table 1, to keep the control loop stable.

DEVICE SETUP AND CONFIGURATION

Table 1. Crystal Frequency Selection and Device Settings

DESIRED OUTPUT FREQUENCY (MHz)		REQUIRED INPUT CRYSTAL FREQUENCY (MHz)		VCO SELECTION	OUTPUT DIVIDER	PRESCALER SETTING	FEEDBACK DIVIDER (1)
From	To	From	To				
1020.0	1175.0	31.875	36.719	VCO 2	1	2	32
875.2 (2)	1020.0	27.351	31.875	VCO 1	1	2	32
650.0	**766.7** (2)	32.500	38.333	VCO 2	1	3	20
583.5	650.0	29.174	32.500	VCO 1	1	3	20
510.0	587.5	31.875	36.719	VCO 2	1	4	16
437.6	510.0	27.351	31.875	VCO 1	1	4	16
408.0	460.0	34.000	38.333	VCO 2	1	5	12
350.1	408.0	29.174	34.000	VCO 1	1	5	12
340.0	383.3	34.000	38.333	VCO 2	2	3	20
291.7	340.0	29.174	34.000	VCO 1	2	3	20
255.0	293.8	31.875	36.719	VCO 2	2	4	16
218.8	255.0	27.351	31.875	VCO 1	2	4	16
204.0	230.0	34.000	38.333	VCO 2	2	5	12
175.0	204.0	29.174	34.000	VCO 1	2	5	12
170.0	191.7	34.000	38.333	VCO 2	4	3	20
145.9	170.0	29.174	34.000	VCO 1	4	3	20
127.5	146.9	31.875	36.719	VCO 2	4	4	16
109.4	127.5	27.351	31.875	VCO 1	4	4	16
102.0	115.0	34.000	38.333	VCO 2	4	5	12
87.5	102.0	29.174	34.000	VCO 1	4	5	12
85.0	95.8	34.000	38.333	VCO 2	8	3	20
72.9	85.0	29.174	34.000	VCO 1	8	3	20
63.8	73.4	31.875	36.719	VCO 2	8	4	16
54.7	63.8	27.351	31.875	VCO 1	8	4	16
51.0	57.5	34.000	38.333	VCO 2	8	5	12
43.8	51.0	29.174	34.000	VCO 1	8	5	12
42.5	47.9	34.000	38.333	VCO 2	16	3	20
36.5	42.5	29.174	34.000	VCO 1	16	3	20
31.9	36.7	31.875	36.719	VCO 2	16	4	16
27.4	31.9	27.351	31.875	VCO 1	16	4	16
25.5	28.8	34.000	38.333	VCO 2	16	5	12
21.9	25.5	29.174	34.000	VCO 1	16	5	12
21.3	24.0	34.000	38.333	VCO 2	32	3	20
18.2	21.3	29.174	34.000	VCO 1	32	3	20
15.9	18.4	31.875	36.719	VCO 2	32	4	16
13.7	15.9	27.351	31.875	VCO 1	32	4	16
12.8	14.4	34.000	38.333	VCO 2	32	5	12
10.9	12.8	29.174	34.000	VCO 1	32	5	12

(1) The feedback divider is set automatically with respect to the prescaler setting.
(2) Discontinuity in frequency range

DEVICE SETUP EXAMPLE

The following example illustrates the procedure to calculate the required AT-cut crystal frequency needed to generate a desired output frequency.

Assuming the requirement to generate an output frequency of 622.08 MHz, Table 1 shows that the desired output frequency lies between 583.5 and 680 MHz.

DESIRED OUTPUT FREQUENCY (MHz)		REQUIRED INPUT CRYSTAL FREQUENCY (MHz)		VCO SELECTION	OUTPUT DIVIDER	PRESCALER SETTING	FEEDBACK DIVIDER (1)
From	To	From	To				
650.0	**766.7**	32.500	38.333	VCO 2	1	3	20
583.5	650.0	29.174	32.500	VCO 1	1	3	20
510.0	587.5	31.875	36.719	VCO 2	1	4	16

(1) The feedback divider is set automatically with respect to the prescaler setting.

So this means that the device must be configured with:

VCO = **VCO 1**
Output divider = **1**
Prescaler setting = **3**

To determine the right crystal frequency needed to get 622.08 MHz with these settings, substitute values into Equation 1.

$$f_{xtal} = \left(\frac{OutputDivider}{FeedbackDivider}\right) \times f_{out} \qquad f_{xtal} = \left(\frac{1}{20}\right) \times 622.08 = 31.154\ \text{MHz} \tag{2}$$

The AT-cut frequency should be **31.154 MHz** (between 29.174 MHz and 32.500 MHz. as shown in Table 1) .

SERIAL INTERFACE AND CONTROL

The CDCE421 uses a unique Texas Instruments proprietary interface protocol that can be configured and programmed via a single input pin to the device. The architecture enables only writing to the device from this input pin. Reading the content of a register can be achieved by sending a read command on the input pin and monitoring the output pins (LVDS or LVPECL). In a case where the output pins cannot be used to read the content, the software controlling the interface must account for what is written to the EEPROM and when it is programmed. Monitoring the outputs verifies the programming modes, and cycling power on the device verifies that the EEPROM is holding the proper configuration.

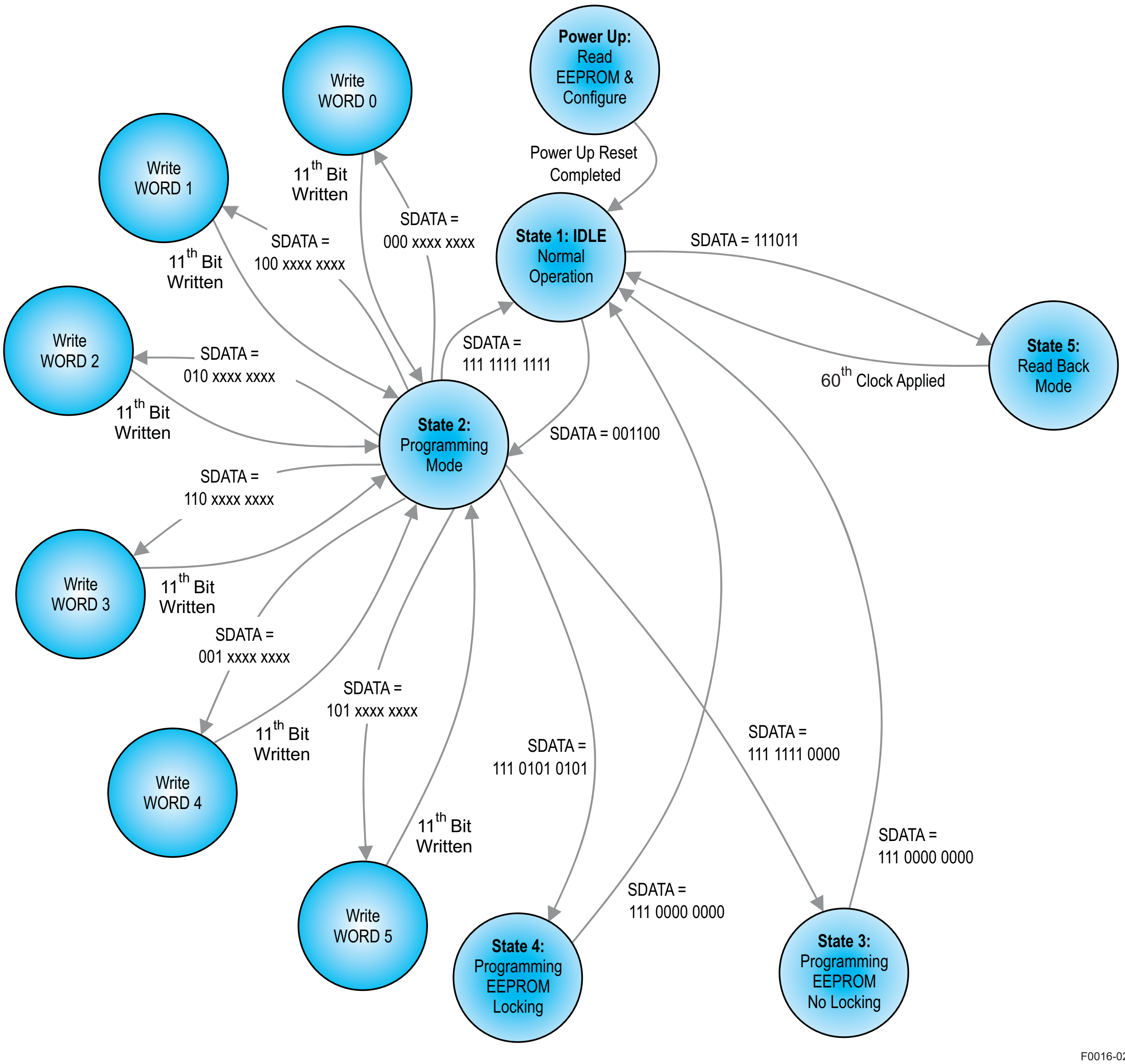
The CDCE421 can be configured and programmed via the SDATA input pin. For this purpose, a square-wave programming sequence must be written to the device as described in the following section. During the EEPROM programming phase, the device requires a stable V_{CC} of 3 V to 3.6 V for secure writing of the EEPROM cells. After each *Write to WordX,* the written data is latched, made effective, and offers look-ahead before the actual data is stored into the EEPROM.

The following table summarizes all valid programming commands.

SDATA	FUNCTION
00 1100	Enter **Programming Mode** (State 1 → State 2); bits must be sent in the specified order with the specified timing. Otherwise, a *time-out* occurs.
11 1011	Enter **Register Read Back Mode**; bits must be sent in the specified order with the specified timing. Otherwise, a *time-out* occurs.
000 xxxx xxxx	**Write to Word0** (State 2) (1) (2) (3)
100 xxxx xxxx	**Write to Word1** (State 2) (1) (2) (3)
010 xxxx xxxx	**Write to Word2** (State 2) (1) (2) (3)

(1) Each rising edge causes a bit to be latched.
(2) Between the bits, some longer time delays can occur, but this has no effect on the data.
(3) A *Write to WordX* is expected to be 10 bits long. After the 10^{th} bit, the respective word is latched and its effect can be observed as *look-ahead* function.

SDATA	FUNCTION
110 xxxx xxxx	**Write to Word3** (State 2)(1) (2) (3)
001 xxxx xxxx	**Write to Word4** (State 2)(1) (2) (3)
101 xxxx xxxx	**Write to Word5** (State 2)(1) (2) (3)
111 xxxx xxxx	**State machine jump:** All other patterns not defined as follows cause an *exit to normal mode.*
111 1111 0000	Jump: **Enter EEPROM programming with EEPROM lock** (State 2 → State 3)
111 0101 0101	Jump: **Enter EEPROM programming without EEPROM lock** (State 2 → State 4)
111 0000 0000	Jump: **Exit EEPROM programming** (State 3 or State 4 → State 1)

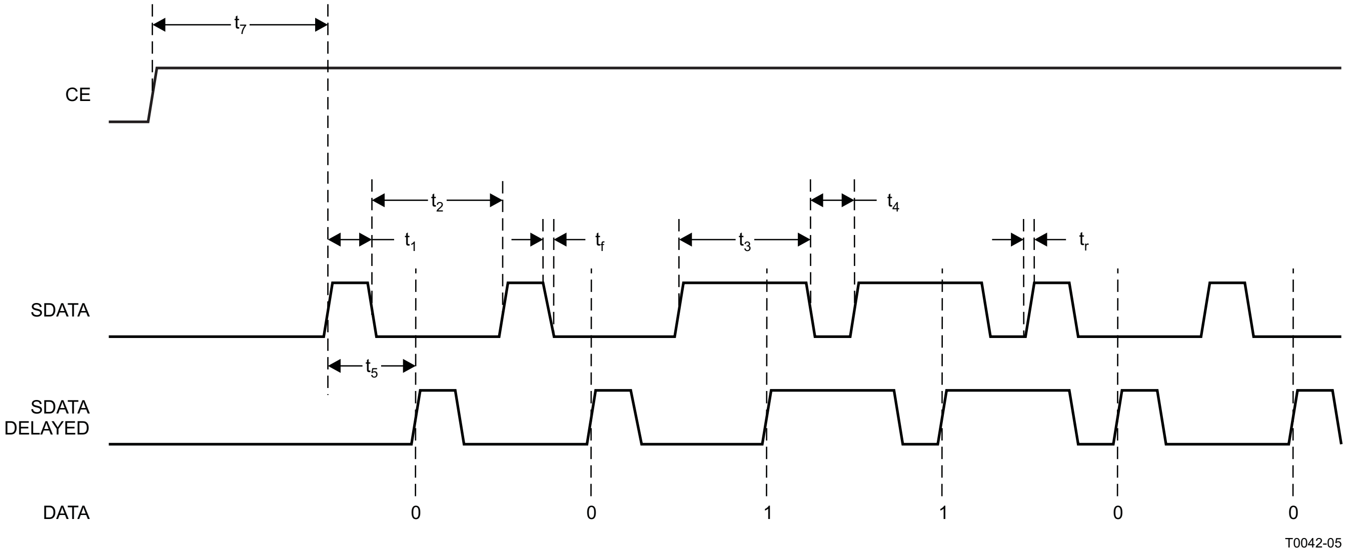


NOTE: In States 2, 3, 4, and 5, the signal pin CE is disregarded and has no influence on power down.

Figure 2. State Flow-Diagram of Single-Pin Interface

Enter *Programming Mode*

Figure 3 shows the timing behavior of data to be written into SDATA. The sequence shown is 00 1100. If the high period is as short as t_1, this is interpreted as 0. If the high period is as long as t_3, this is interpreted as a 1. This behavior is achieved by shifting the incoming signal SDATA by time t_5 into signal SDATA_DELAYED. As can be seen in Figure 3, SDATA_DELAYED can be used to latch (or strobe) SDATA. The timing specifications for t_1–t_7, t_r, and t_f are shown in Figure 3.



		MIN	TYP	MAX	UNIT
$f_{SDATACLK}$	Repeat frequency of programming	60	70	80	kHz
t_1	LOW signal: high-pulse duration		0.2 t		ms
t_2	LOW signal: low-pulse duration while entering programming sequence		0.8 t		ms
t_2	LOW signal: low-pulse duration while programming bits		0.8 t		ms
t_3	HIGH signal: high-pulse duration		0.8 t		ms
t_4	HIGH signal: low-pulse duration while entering programming sequence		0.2 t		ms
t_4	HIGH signal: low-pulse duration while programming bits		0.2 t		ms
t_6	Time-out during *Entering Programming Mode* and *Enter Read Back Mode*. High-pulse or low-pulse duration each must be less than this time; otherwise, time-out will result.	16			µs
t_7	CE-high time before first SDATA can be clocked in	3 t			ms
t_r and t_f	Rise Time and Fall Time		2		ns
$t = 1 / f_{SDATACLK}$					

Figure 3. SDATA/CE Timing

EEPROM PROGRAMMING

Load all the registers in RAM by writing Word0 through Word5, and after going back to State 2, then going to State 3 (programming EEPROM, no locking) or State 4 (programming EEPROM with locking), the contents of Word0–Word5 are saved in the EEPROM. Wait 10 ms in State 3 or State 4 when programming the EEPROM before moving to State 2 (the idle state).

NOTE:

When writing to the device for functionality testing and verification via the serial bus, only the RAM is being accessed.

EXAMPLE: Programming Cycle of Six Words and Programming Into EEPROM

The following sequence shows how to *enter programming mode* and how the different words can be written. The addressing of Word0 … Word5 is shown in bold. After the word address, the payload for the respective word is clocked in. In this example, this is followed by a jump from State 2 → State 3 into *enter EEPROM programming with EEPROM lock*. In the EEPROM-programming state, it is necessary to wait at least 10 ms for safe programming. The last command is a jump from State 3 into State 1 (normal operation). Cycle power and verify that the device functions as programmed.

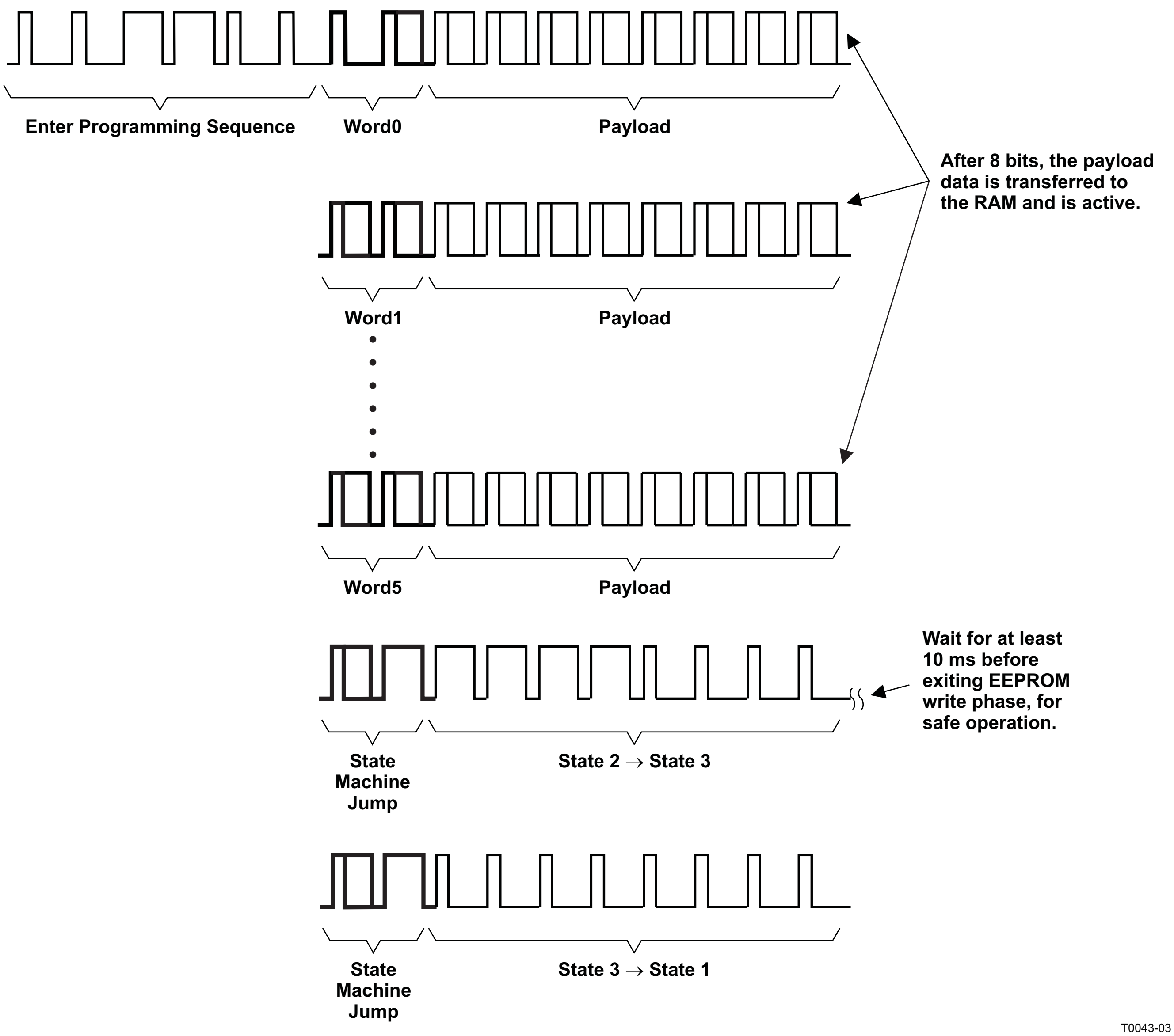
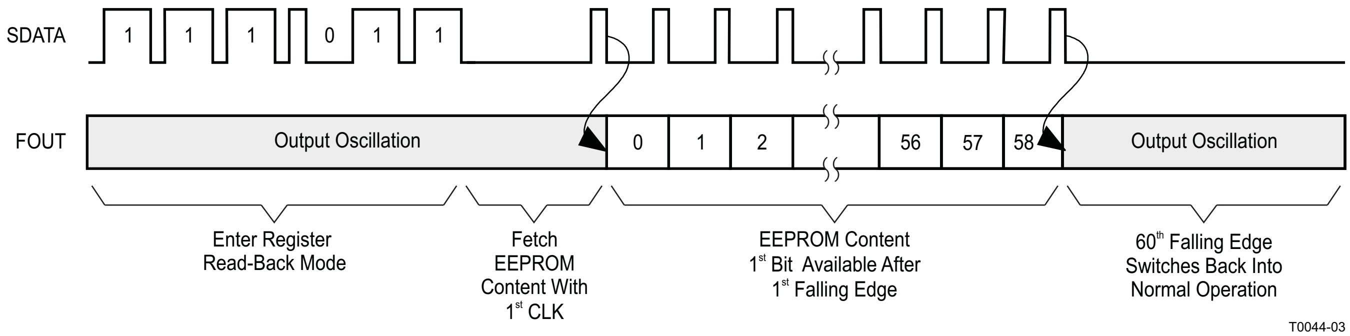


Figure 4. Programming Cycle of Six Words and Programming Into EEPROM

Enter *Register Readback Mode* and Related Timing Diagram

Similar to the *enter programming mode* sequence, the *enter register read back mode* is written into SDATA. After the command has been issued, the SDATA input is reconfigured as clock input. By applying one clock, the EEPROM content is read into shift registers. Now, by further applying clocks at SDATA, the EEPROM content can be clocked out and observed at OUTP/OUTN. There are 59 bits to be clocked out. With the 61st rising clock edge, the OUTP/OUTN pins are reconfigured back into normal operation.



In the following table, the content of the output bit stream is summarized. Important to notice: bit 0 is clocked out first. The Default values in register 0 to register 5 are programmed in the EEPROM.

OUTPUT BIT STREAM	FUNCTION
Bits[0:2]	Revision identifier (MSB first)
Bits[3:8]	VCO calibration word
Bit[9]	EEPROM status: 0 = EEPROM has never been written 1 = EEPROM has been programmed before
Bit[10]	EEPROM lock: 0 = EEPROM can be rewritten 1 = EEPROM is locked, rewriting to the EEPROM is not possible any more
Bits[11:18]	Storage value, Word5 (MSB first)
Bits[19:26]	Storage value, Word4 (MSB first)
Bits[27:34]	Storage value, Word3 (MSB first)
Bits[35:42]	Storage value, Word2 (MSB first)
Bits[43:50]	Storage value, Word1 (MSB first)
Bits[51:58]	Storage value, Word0 (MSB first)

REGISTER DESCRIPTION

Word 0:

BIT	NAME	DESCRIPTION/FUNCTION	TYPE	DEFAULT VALUE
0	C0	Register selection	W	0
1	C1	Register selection	W	0
2	C2	Register selection	W	0
3	SELVCO	VCO select, 0 = VCO1, 1 = VCO2	W	0
4	SELPRESC	Prescaler setting, bit 0	W	0
5	SELPRESC	Prescaler setting, bit 1	W	1
6	OUTSEL	Output divider select, bit 0	W	1
7	OUTSEL	Output divider select, bit1	W	1
8	OUTSEL	Output divider select, bit 2	W	0
9	DRVSEL	Driver select, 0 = LVDS, 1 = PECL	W	1
10	ILFSEL	Loop filter bias select	W	0

4	Divide by value (SELPRESC 1, SELPRESC 0) Divide by 5 = (00), 3 = (01), 4 = (10), 2 = (11)
5	
6	Output divider (OUTSEL2, OUTSEL1, OUTSEL0) Divide by 1 = (000), 2 = (001), 4 = (010), 8 = (011), 16 = (100), 32 = (101)
7	
8	

Word 1:

BIT	NAME	DESCRIPTION/FUNCTION	TYPE	DEFAULT VALUE
0	C0	Register selection	W	1
1	C1	Register selection	W	0
2	C2	Register selection	W	0
3	LFRCSEL	Loop filter control settings, bit 0	W	1
4	LFRCSEL	Loop filter control settings, bit 1	W	1
5	LFRCSEL	Loop filter control settings, bit 2	W	1
6	LFRCSEL	Loop filter control settings, bit 3	W	1
7	LFRCSEL	Loop filter control settings, bit 4	W	1
8	LFRCSEL	Loop filter control settings, bit 5	W	0
9	LFRCSEL	Loop filter control settings, bit 6	W	1
10	LFRCSEL	Loop filter control settings, bit 7	W	0

Word 2:

BIT	NAME	DESCRIPTION/FUNCTION	TYPE	DEFAULT VALUE
0	C0	Register selection	W	0
1	C1	Register selection	W	1
2	C2	Register selection	W	0
3	LFRCSEL	Loop filter control settings, bit 8	W	1
4	LFRCSEL	Loop filter control settings, bit 9	W	1
5	LFRCSEL	Loop filter control settings, bit 10	W	0
6	LFRCSEL	Loop filter control settings, bit 11	W	0
7	LFRCSEL	Loop filter control settings, bit 12	W	0
8	LFRCSEL	Loop filter control settings, bit 13	W	0
9	LFRCSEL	Loop filter control settings, bit 14	W	0
10	LFRCSEL	Loop filter control settings, bit 15	W	0

Word 3:

BIT	NAME	DESCRIPTION/FUNCTION	TYPE	DEFAULT VALUE
0	C0	Register selection	W	1
1	C1	Register selection	W	1
2	C2	Register selection	W	0
3	LFRCSEL	Loop filter control settings, bit 16	W	0
4	LFRCSEL	Loop filter control settings, bit 17	W	0
5	LFRCSEL	Loop filter control settings, bit 18	W	0
6	ICPSEL	Charge pump current sel, bit 0	W	1
7	ICPSEL	Charge pump current sel, bit 1	W	1
8	ICPSEL	Charge pump current sel, bit 2	W	1
9	ICPSEL	Charge pump current sel, bit 3	W	1
10	Not Used		W	0

Word 4:

BIT	NAME	DESCRIPTION/FUNCTION	TYPE	DEFAULT VALUE
0	C0	Register selection	W	0
1	C1	Register selection	W	0
2	C2	Register selection	W	1
3	CALWRD	VCO calibration word, bit 0	W	0
4	CALWRD	VCO calibration word, bit 1	W	0
5	CALWRD	VCO calibration word, bit 2	W	0
6	CALWRD	VCO calibration word, bit 3	W	0
7	CALWRD	VCO calibration word, bit 4	W	0
8	CALWRD	VCO calibration word, bit 5	W	0
9	CALOVR	VCO calibration override	W	0
10	ENCAL	Enable VCO calibration	W	1

Word 5:

BIT	NAME	DESCRIPTION/FUNCTION	TYPE	DEFAULT VALUE
0	C0	Register selection	W	1
1	C1	Register selection	W	0
2	C2	Register selection	W	1
3	TITSTCFG	TI test use, bit 0	W	0
4	TITSTCFG	TI test use, bit 1	W	0
5	TITSTCFG	TI test use, bit 2	W	0
6	TITSTCFG	TI test use, bit 3	W	0
7	Not used		W	0
8	Not used		W	0
9	Not used		W	0
10	Not used		W	0

PACKAGE (DIE)

The CDCE421 is available in die form or in a QFN 24-pin package. The die version pad locations and numbers are shown in Figure 5.

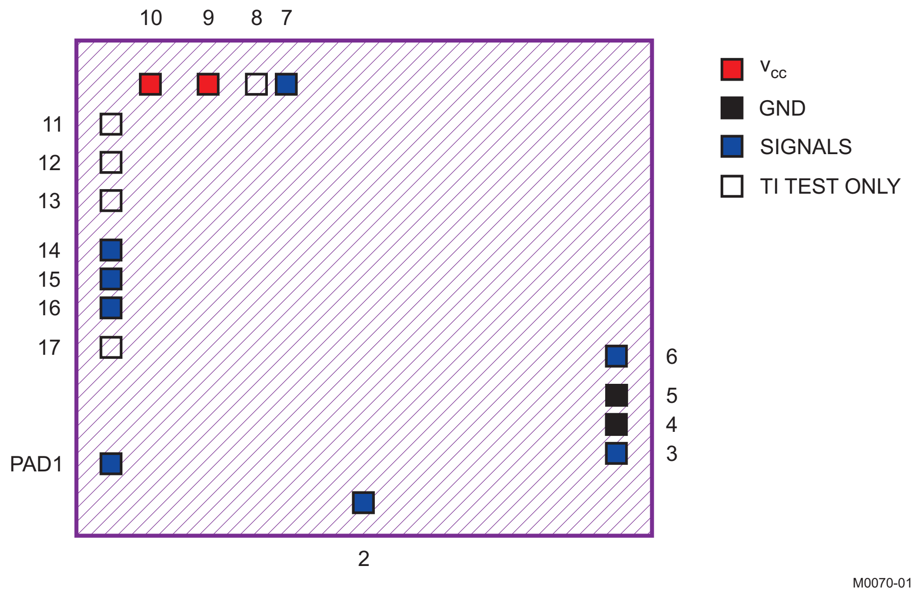


Figure 5. Pinout of the CDCE421 Die

PAD DESCRIPTION

Table 2 shows the pin description for the CDCE421 die.

Table 2. Pad Description of CDCE421 (See Appendix B for More Information)

TERMINAL NAME	PAD NO.	TYPE	ESD Protection	Description
CE	1	O	Y	Chip enable CE = 1: enable the device and the outputs. CE = 0: disable all current sources; in LVDS mode, LVDSP = LVDSN = Hi-Z; in LVPECL mode, LVPECLP = LVPECLN = Hi-Z.
OUTN	3	O	Y	High-speed negative differential LVPECL or LVDS outputs. (Outputs are enabled by CE and selected by the EEPROM configuration registers.)
OUTP	6	O	Y	High-speed positive differential LVPECL or LVDS outputs. (Outputs are enabled by CE and selected by the EEPROM configuration registers.)
SDATA	2	I	Y	Programming pin using TI proprietary interface protocol
Test pins	7, 8, 11–13, 16, 17			Do not connect (TI Manufacturing test pins).
V_{CC}	9, 10	Power	Y	3.3-V power supply
V_{SS}	4, 5	GND	Y	Ground
XIN 1	14	I	Y	Connect XIN1 to one end of the crystal and XIN2 to the other end of the crystal.
XIN 2	15	I	N	

PACKAGE (QFN24)

The CDCE421 is also packaged in a QFN 24-pin package. The QFN package footprint is shown. Pad locations and numbers are shown in Figure 6.

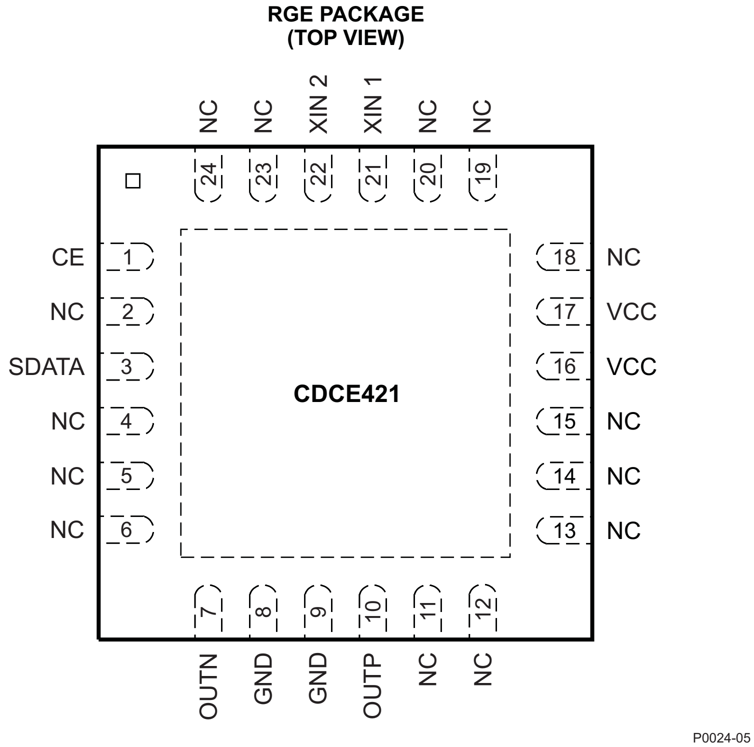


Figure 6. Pinout of the CDCE421 QFN-24 Package

PIN DESCRIPTION

Table 3 shows the pin description for the CDCE421 QFN-24 Package.

Table 3. Pinout Description of CDCE421

TERMINAL NAME	TERMINAL NO.	TYPE	ESD Protection	Description
CE	1	I	Y	Chip enable CE = 1: enable the device and the outputs. CE = 0: disable all current sources; in LVDS mode, LVDSP = LVDSN = Hi-Z; in LVPECL mode, LVPECLP = LVPECLN = Hi-Z.
GND	8, 9	GND	Y	Ground
No connect	2, 4–6, 11–15, 18–20, 23,24			Do not connect these pins. Leave them floating.
OUTN	7	O	Y	High-speed negative differential LVPECL or LVDS outputs. (Outputs are enabled by CE and selected by the EEPROM configuration registers.)
OUTP	10	O	Y	High-speed positive differential LVPECL or LVDS outputs. (Outputs are enabled by CE and selected by the EEPROM configuration registers.)
SDATA	3	I	Y	Programming pin using TI proprietary interface protocol
VCC	16, 17	Power	Y	3.3-V power supply
XIN 1 XIN 2	21 22	I GND/NC	Y N	In crystal input mode, connect XIN1 to one end of the crystal and XIN2 to the other end of the crystal. In LVCMOS input single-ended driven mode, XIN1 (pin 21) acts as an input reference, and XIN2 should connect to GND or it can be left unconnected.

OUTPUTS (LVPECL OR LVDS)

The CDCE421 device has two sets of output drivers, LVPECL and LVDS, where the outputs are wire-ORed together. Only one output can be selected at a time; the other goes to the high-impedance state (Hi-Z).

If the device is configured for an LVPECL, the output buffers go to Hi-Z and the termination resistors determine the state of the output (LVPECLP = LVPECLN = Hi-Z) in the device disable mode (CE = L). If the device is configured in LVDS mode, the outputs go to Hi-Z if the device is disabled (CE = L).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{CC}	Supply voltage (2)	–0.5 to 4.6	V
V_I	Voltage range for all other input pins (2)	–0.5 to V_{CC} + 0.5	V
I_O	Output current for LVPECL	–50	mA
	Electrostatic discharge (HBM)	2	kV
T_A	Characterized free-air temperature range (no airflow)	–40 to 85	°C
T_J	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Ambient temperature (no airflow, no heat sink)	–40		85	°C

ELECTRICAL CHARACTERISTICS

recommended operating conditions for CDCE421 device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
$I_{VCC(LVDS)}$	Total current	LVDS mode, 3.3 V, 366 MHz		73	93	mA
$I_{VCC(LVPECL)}$	Total current consumption	LVPECL mode, 3.3 V, 366 MHz		91	110	mA
LVDS OUTPUT MODE (see Figure 10)						
f_{CLK}	Output frequency		10.9		400	MHz
$\|V_{OD}\|$	LDVS differential output voltage	R_L = 100 Ω	240	400	454	mV
ΔV_{OD}	LVDS VOD magnitude change				50	mV
V_{OS}	Offset voltage	–40°C to 85°C	0.84	1.1	1.39	V
ΔV_{OS}	VOS magnitude change				25	mV
t_r	Output rise time	20% to 80% of V_{OUTpp}		170		ps
t_f	Output fall time	80% to 20% of V_{OUTpp}		170		ps
I_{OS}	Short-circuit output current	Short V_{out+} to ground			–20	mA
		Short V_{out-} to ground			20	mA
	Duty cycle of the output waveform		46%	50%	53%	

ELECTRICAL CHARACTERISTICS (continued)

recommended operating conditions for CDCE421 device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL OUTPUT MODE (see Figure 11)						
f_{CLK}	Output frequency		10.9		1175	MHz
V_{OH}	LVPECL high-level output voltage		V_{CC} – 1.2		V_{CC} – 0.81	V
V_{OL}	LVPECL low-level output voltage		V_{CC} – 2.17		V_{CC} – 1.36	V
$\|V_{OD}\|$	LVPECL differential output voltage		407		1076	mV
t_r	Output rise time	20% to 80% of V_{OUTpp}		170		ps
t_f	Output fall time	80% to 20% of V_{OUTpp}		170		ps
	Duty cycle of the output waveform		45%		55%	
	Duty cycle exception	630 MHz to 650 MHz	43%		57%	
LVCMOS INPUT						
$V_{IL,CMOS}$	Low-level CMOS input voltage	V_{CC} = 3.3 V			0.3 V_{CC}	V
$V_{IH,CMOS}$	High-level CMOS input voltage	V_{CC} = 3.3 V	0.7 V_{CC}			V
$I_{L,CMOS}$	Low- level CMOS input current	V_{CC} = V_{CC} max, V_{IL} = 0 V			–200	µA
$I_{H,CMOS}$	High-level CMOS input current	V_{CC} = V_{CC} min, V_{IH} = 3.7 V			200	µA

JITTER CHARACTERISTICS IN INPUT CLOCK MODE

The jitter characterization test is performed using an LVCMOS input signal driving a CDCE421 device packaged in the QFN-24 package.

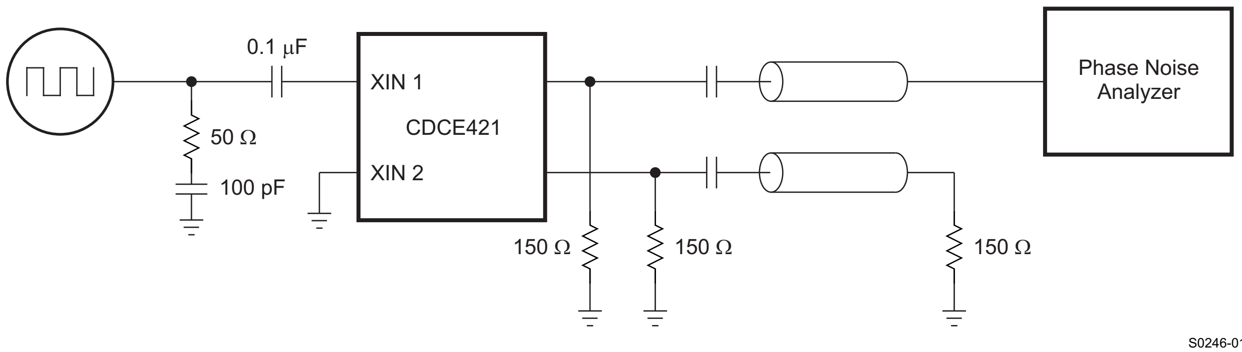


Figure 7. Jitter Test Configuration for an LVTTL Input Driving the CDCE421

Table 4. Measured Output Jitter

					LVPECL (Typical Measured Output Jitter), ps			LVDS (Typical Measured Output Jitter), ps		
Output Frequency (MHz)	Input Frequency (MHz)	VCO	Pre-scaler	Divider	JRMS (12 kHz to 20 MHz)	Tj (Total Jitter)	Dj (Deterministic Jitter)	JRMS (12 kHz to 20 MHz)	Tj (Total Jitter)	Dj (Deterministic Jitter)
100	33.3333	1	5	4	0.507	35.33	11.54	0.552	41.86	21.4
106.25	35.4167	2	5	4	0.53	30.39	11	0.564	35.38	16.01
125	31.25	1	4	4	0.529	47.47	25.2	0.561	74.14	53.51
156.25	31.25	1	3	4	0.472	31.54	9.12	0.482	42.31	23.33
212.5	35.4167	2	5	2	0.512	33.96	13.78	0.523	58.45	37.84
250	31.25	1	4	2	0.42	36.98	18.52	0.525	87.5	67.35
312.5	31.25	1	3	2	0.378	29.82	11	0.45	66.44	47.49
370	30.8333	1	5	1	0.369	29.6	12.05	0.439	69.77	51.2
400	33.3333	1	5	1	0.377	28.1	11.48	0.501	69.75	51.87
708	35.4	2	3	1	0.438	31.65	14.84			
1000	31.25	1	2	1	0.456	40.34	19.66			

If the CDCE421 is being referenced by an external and cleaner LVCMOS input of 35.42 MHz, Figure 8 shows the SSB phase noise plot of the output at 708 MHz from 100 Hz to 40 MHz from the carrier. Note the dependence of output jitter on the input reference jitter. See Figure 13 for test setup.

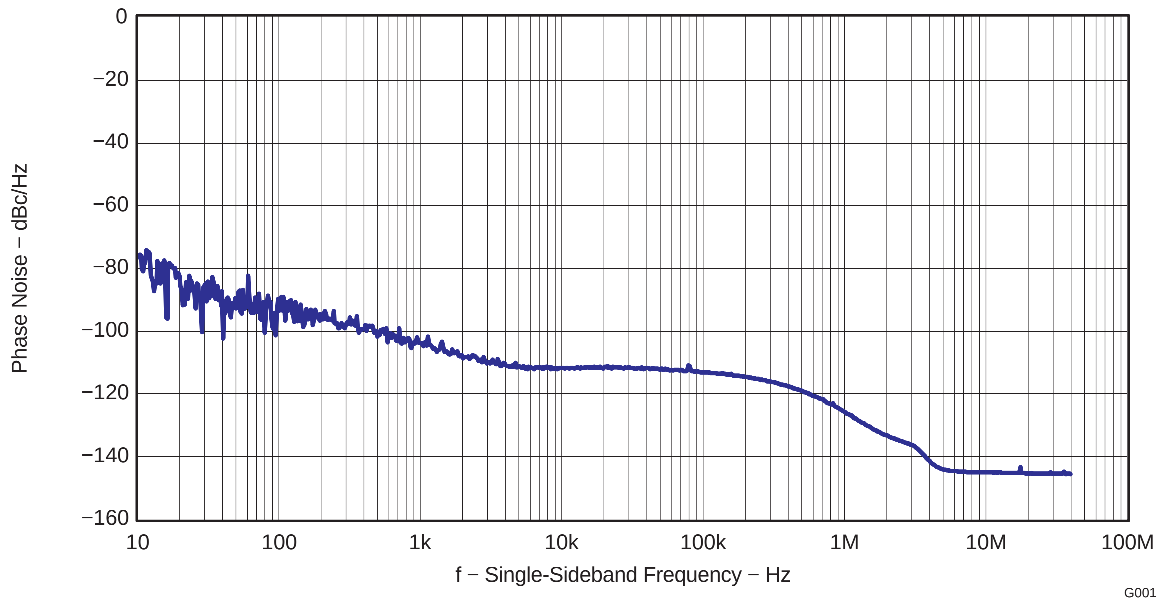


Figure 8. Phase Noise Plot for LVPECL Output at 708 MHz

Table 5. Phase Noise Parameters With LVCMOS Input of 35.4 MHz and LVPECL Output at 708 MHz

Phase noise specifications under following assumptions: input frequency f = 35.42 MHz (VCO = 2, prescaler = 3, output divider = 1), f_{out} = 708 MHz (driver mode = LVPECL)					
PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz		–95		dBc/Hz
phn_{1k}	Phase noise at 1 kHz		–105		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–109		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–114		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–126		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–146		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–146		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		438		fs

If the CDCE421 is being referenced by a clean external LVCMOS input of 33.33 MHz, Figure 9 shows the SSB phase noise plot of the output at 400 MHz from 100 Hz to 40 MHz from carrier. See Figure 12 for test setup.

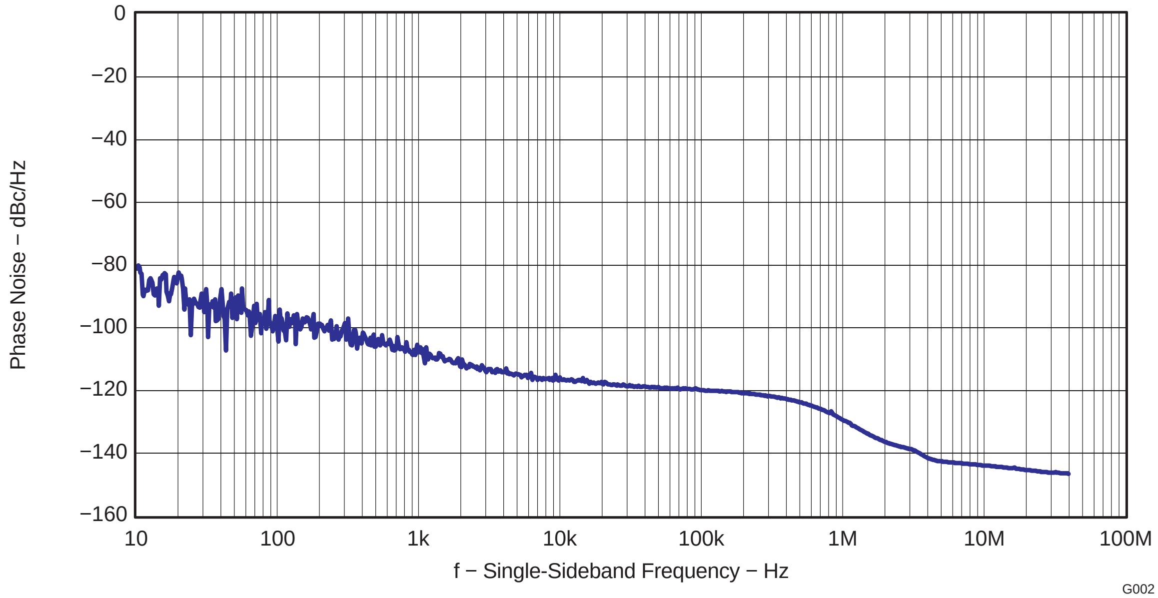


Figure 9. Phase Noise Plot for LVDS Output at 400 MHz

Table 6. Phase Noise Parameters With LVCMOS Input of 33.33 MHz and LVDS Output at 400 MHz

Phase noise specifications under following assumptions: input frequency f = 33.33 MHz (VCO = 1, prescaler = 5, output divider = 1), f_{out} = 400 MHz (driver mode = LVDS)					
PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz		–99		dBc/Hz
phn_{1k}	Phase noise at 1 kHz		–107		dBc/Hz
phn_{10k}	Phase noise at 10 kHz		–115		dBc/Hz
phn_{100k}	Phase noise at 100 kHz		–119		dBc/Hz
phn_{1M}	Phase noise at 1 MHz		–128		dBc/Hz
phn_{10M}	Phase noise at 10 MHz		–144		dBc/Hz
phn_{20M}	Phase noise at 20 MHz		–145		dBc/Hz
J_{RMS}	RMS jitter integrated from 12 kHz to 20 MHz		501		fs

APPENDIX A: TEST CONFIGURATIONS

Test setups are used to characterize the CDCE421 device in ac and dc terminations. The following figures illustrate all four setups used to terminate the clock signal driven by the device under test.

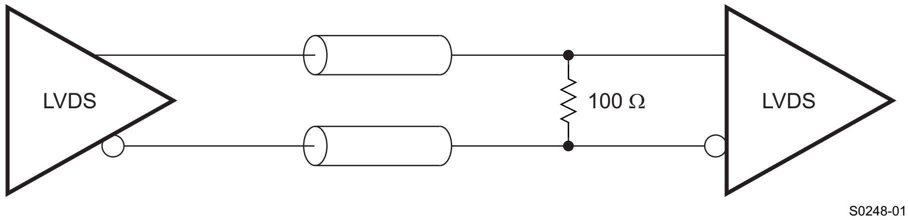


Figure 10. LVDS DC Termination Test Configuration

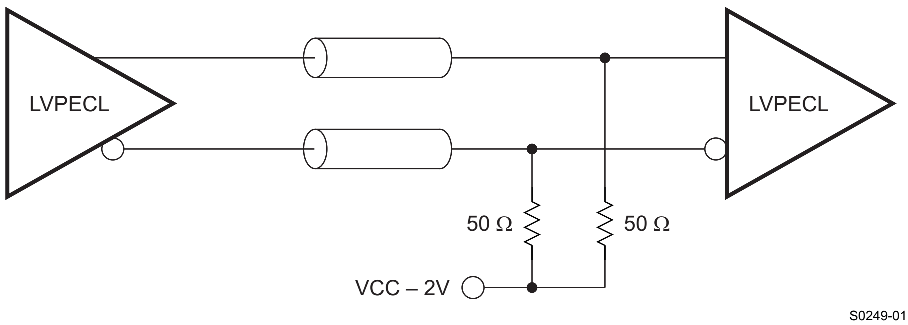


Figure 11. LVPECL DC Termination Test Configuration

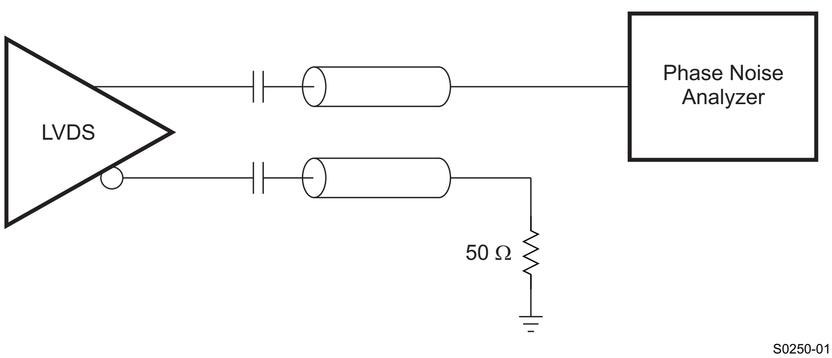


Figure 12. LVDS AC Termination Test Configuration

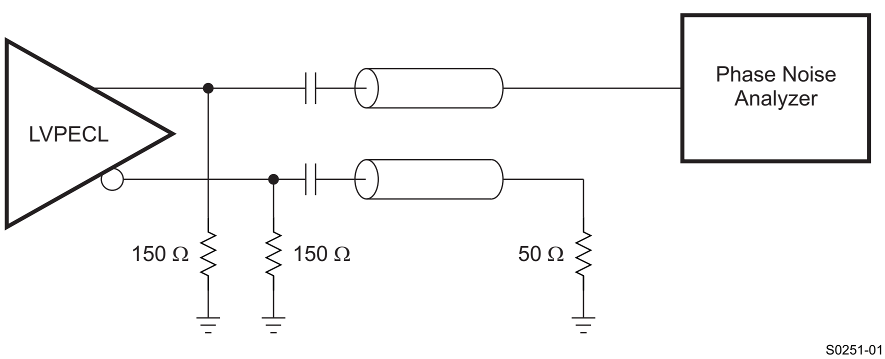
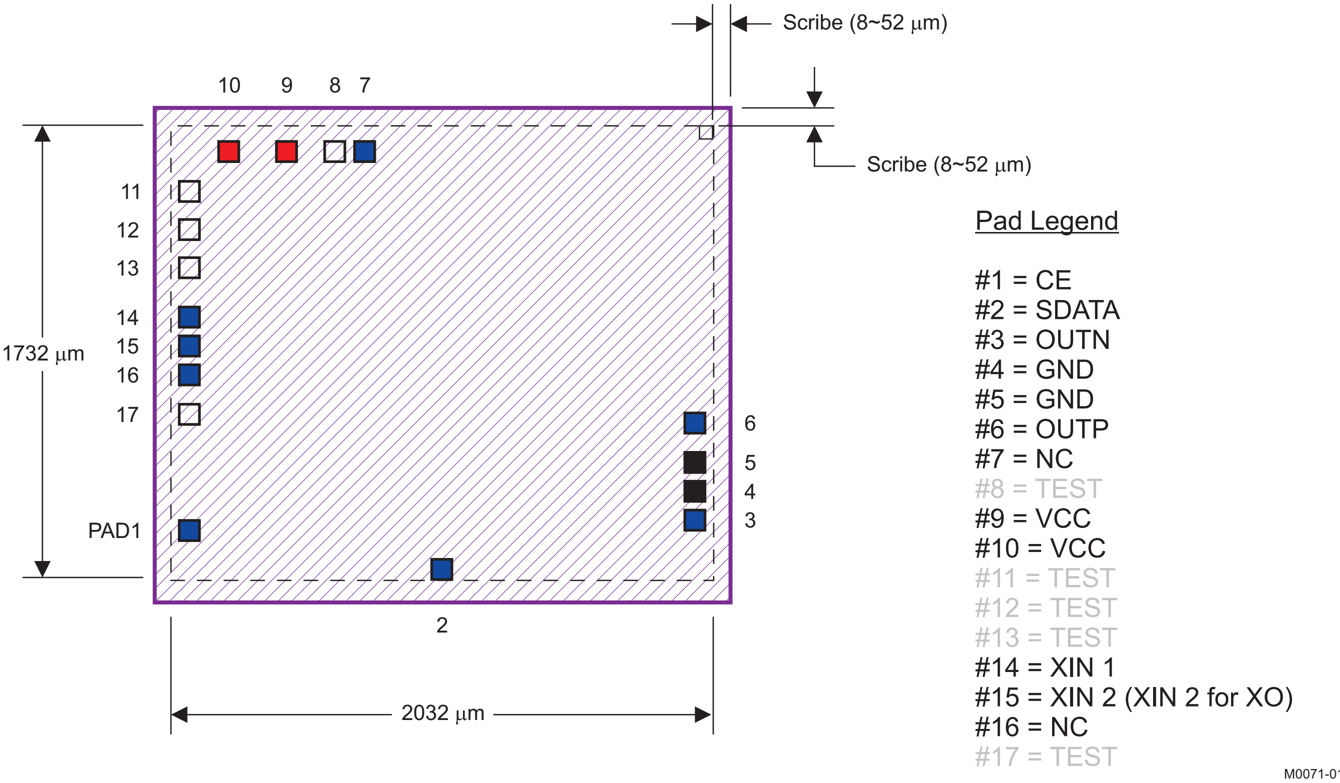


Figure 13. LVPECL AC Termination Test Configuration

APPENDIX B: PACKAGE

Packaging and bond wiring the CDCE421 is the responsibility of the oscillator vendor.



PAD	X1	Y1	X2	Y2
1	41.85	198.65	111.85	268.65
2	990.07	48.65	1060.07	118.65
3	1918.35	237.28	1988.35	307.28
4	1917.93	355.14	1987.93	425.14
5	1922.2	456.66	1992.2	526.66
6	1917.86	573.58	1987.86	643.58
7	714.86	1619.99	784.86	1689.99
8	595.74	1620.25	665.74	1690.25
9	392.97	1621.07	462.97	1691.07
10	198.04	1620.76	268.04	1690.76
11	41.9	1469.91	111.9	1539.91
12	42.19	1310.51	112.19	1380.51
13	42.35	1154.46	112.35	1224.46
14	41.97	993.15	111.97	1063.15
15	42.84	881.73	112.84	951.73
16	41.87	771.71	111.87	841.71
17	41.87	617.6	111.87	687.6

The CDCE421 is designed to be mounted in a commonly used 6-pin oscillator package, where pin 2 (N/C) is the programming pin, in conjunction with CE for the XO design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDCE421RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCE421RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCE421RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCE421RGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CDCE421Y	ACTIVE	DIESALE	Y	0	182	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type
CDCE421YS	ACTIVE	WAFER SALE	YS	0	30635	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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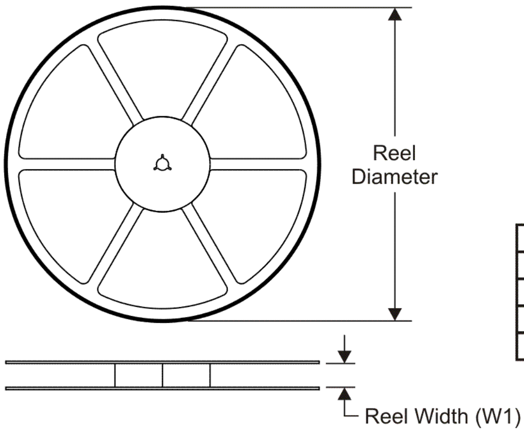
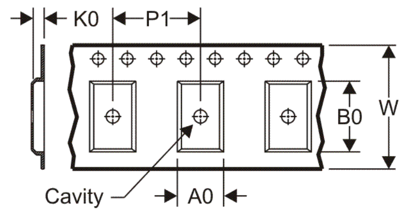
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

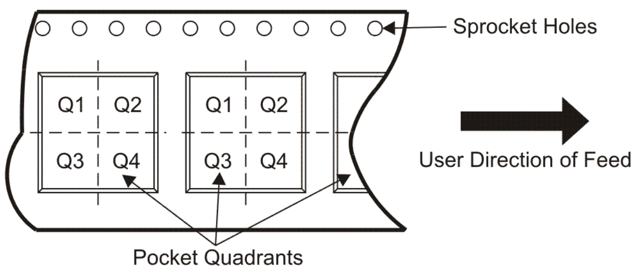


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

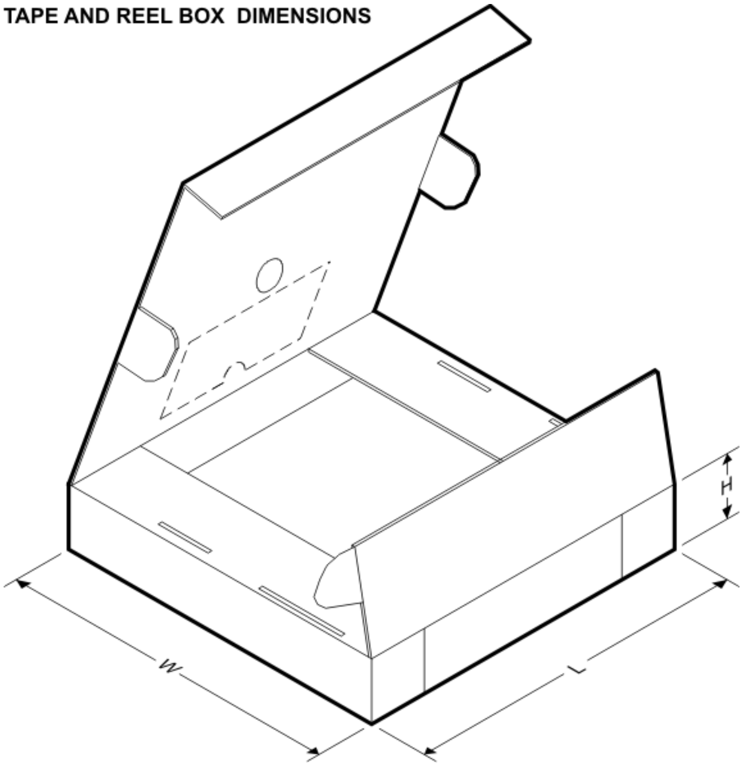
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE421RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CDCE421RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

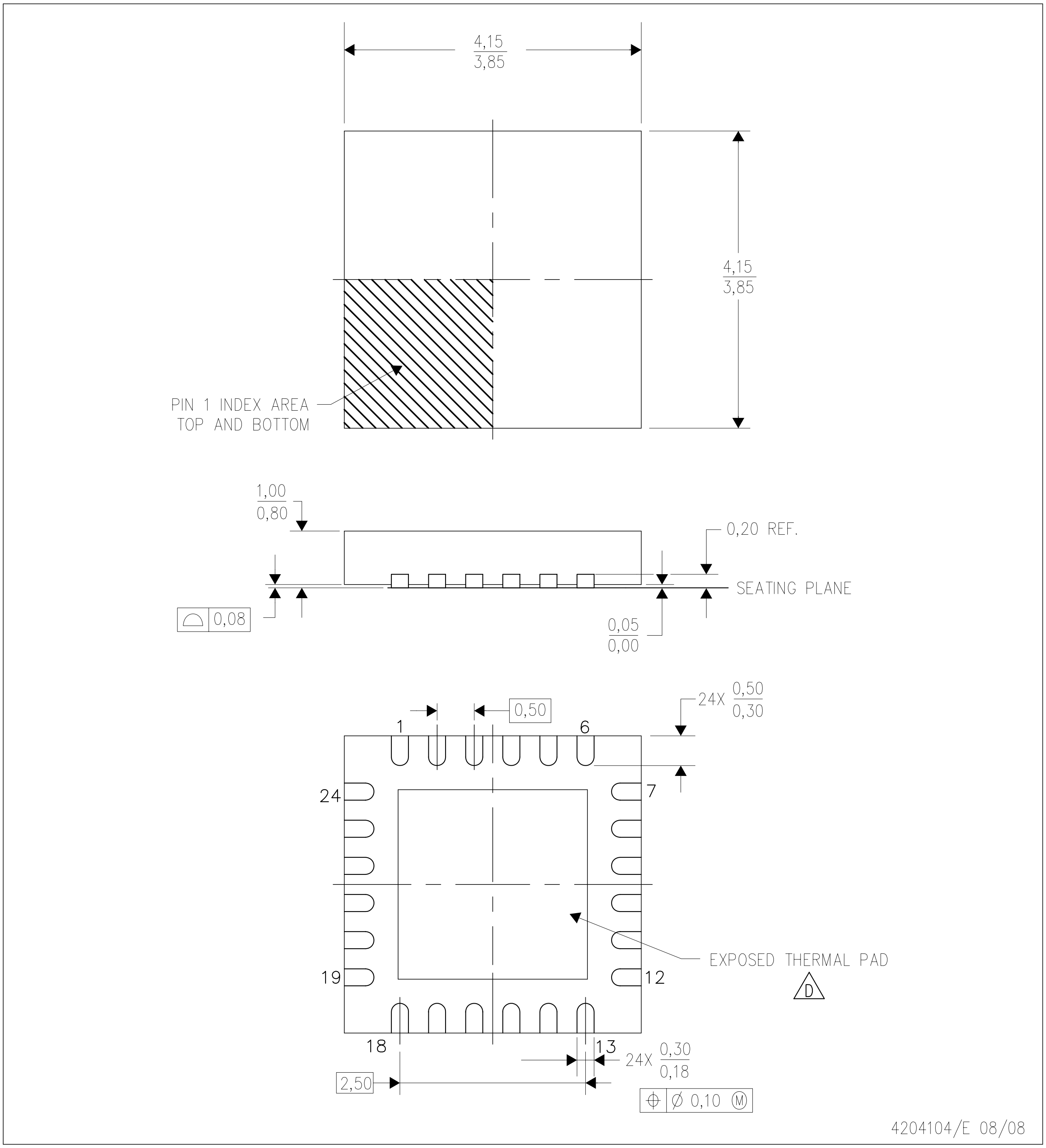
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE421RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
CDCE421RGET	VQFN	RGE	24	250	190.5	212.7	31.8

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

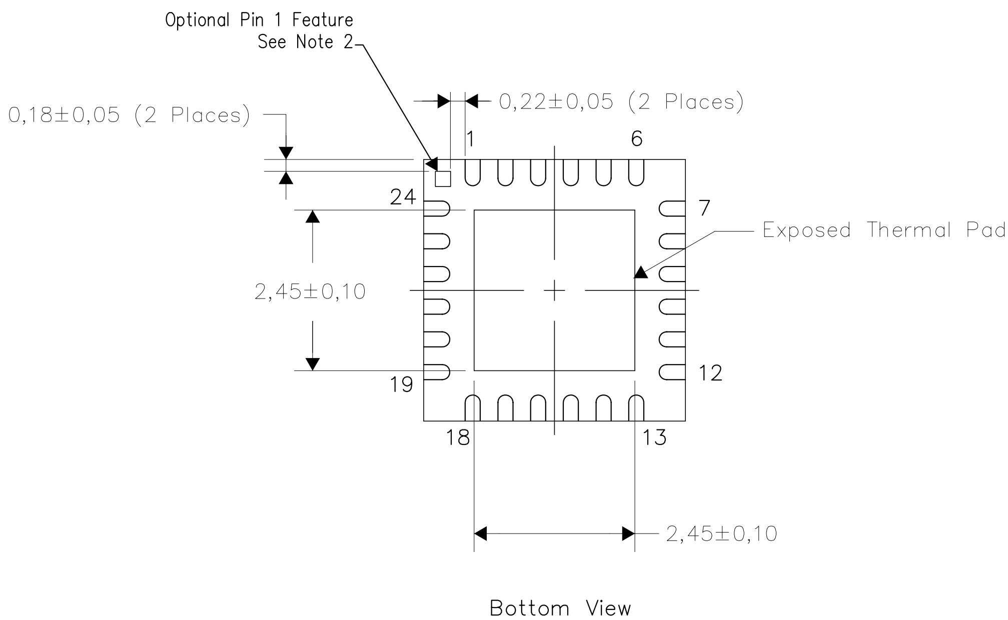
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No—Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO—220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

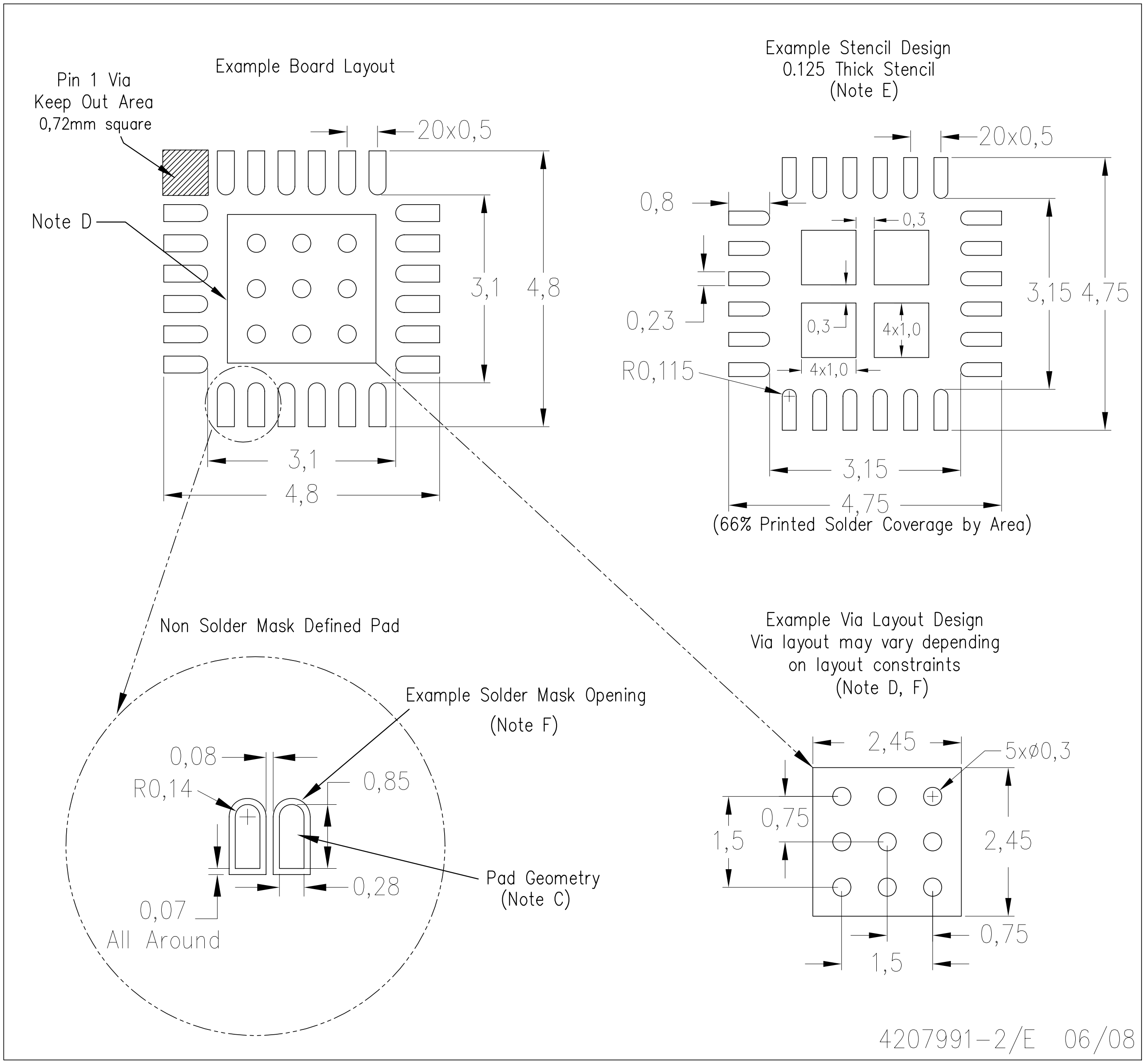
The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

NOTES:
1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices
In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S-PVQFN-N24)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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